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AN INTERCONNECT AND A METHOD OF MANUFACTURE THEREFOR

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TECHNICAL FIELD OF THE INVENTION

[0001] The present invention is directed, in general, to an interconnect and, more specifically, to an interconnect including a surface conductive lead, a method of manufacture therefor, and a method for manufacturing an integrated circuit including the surface conductive lead.

BACKGROUND OF THE INVENTION

[0002] For integrated circuit power devices that experience high currents, *e.g.*, currents above about 100 milliamps, thick copper is desirable for forming low resistance leads. Where the currents are above about 1 amp, and especially when the currents are above about 10 amps, thick copper can be considered essential. Thick copper allows the higher currents to be carried in a considerably smaller area than would be required with other metal layers. Thick copper is formed over a protective overcoat. The protective overcoat provides physical, chemical, and ion protection for underlying structures.

[0003] According to a standard process for forming thick copper leads, the protective overcoat is lithographically patterned to

expose the bond pads. The bond pads are typically about 60 μm to about 100 μm square. A conductive barrier layer and a copper seed layer are sputter deposited over the protective overcoat and within the openings patterned through the overcoat. A resist coating is then formed and patterned to cover the copper seed layer everywhere except where thick copper is desired. Thick copper is then plated on the surface. After plating, the resist is removed and exposed portions of the barrier layer and seed layer are etched away using a wet etchant. This process is generally effective, but the resulting products in some cases may show undesirable failure rates, especially in next generation devices.

[0004] Accordingly, what is needed in the art is an improved interconnect lead and a method of manufacture therefor.

SUMMARY OF THE INVENTION

[0005] To address the above-discussed deficiencies of the prior art, the present invention provides an interconnect for use in an integrated circuit, a method for manufacturing the interconnect, and a method for manufacturing an integrated circuit including the interconnect. The interconnect for use in the integrated circuit, among other elements, includes a surface conductive lead located in an opening formed within a protective overcoat, and a barrier layer located between the protective overcoat and the surface conductive lead, a portion of the barrier layer forming a skirt that extends outside a footprint of the surface conductive lead.

[0006] The method for manufacturing the interconnect, among other steps, includes forming a surface conductive lead in an opening formed within a protective overcoat and over a barrier layer, a portion of the barrier layer extending beyond the surface conductive lead, and subjecting the portion of the barrier layer to a dry etch to remove the portion, the dry etch selective to the barrier layer.

[0007] The foregoing has outlined preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the

invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The invention is best understood from the following detailed description when read with the accompanying FIGUREs. It is emphasized that in accordance with the standard practice in the semiconductor industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion. Reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0009] FIGURE 1 illustrates a cross-sectional view of one embodiment of an interconnect system manufactured in accordance with the principles of the present invention;

[0010] FIGURE 2 illustrates a cross-sectional view of a partially completed interconnect system;

[0011] FIGURE 3 illustrates a cross-sectional view of the partially completed interconnect system illustrated in FIGURE 2 after forming a barrier layer over the protective overcoat and within the opening;

[0012] FIGURE 4 illustrates a cross-sectional view of the partially completed interconnect system illustrated in FIGURE 3 after forming a seed layer over the barrier layer and within the opening;

[0013] FIGURE 5A illustrates a cross-sectional view of the

partially completed interconnect system illustrated in FIGURE 4 after patterning a thick resist layer over the protective overcoat and forming a surface conductive lead within the opening patterned in the resist layer;

[0014] FIGURE 5B illustrates a cross-sectional view of an alternative embodiment of the partially completed interconnect system illustrated in FIGURE 5A after forming optional protective layers over the top surface of the surface conductive lead;

[0015] FIGURE 6 illustrates a cross-sectional view of the partially completed interconnect system illustrated in FIGURE 5B after removing the thick resist layer and etching the exposed portions of the seed layer to form an etched seed layer;

[0016] FIGURE 7 illustrates a cross-sectional view of the partially completed interconnect system illustrated in FIGURE 6 after etching portions of the barrier layer extending beyond the surface conductive lead to form a completed interconnect system; and

[0017] FIGURE 8 illustrates an exemplary cross-sectional view of a conventional integrated circuit (IC) incorporating an interconnect system constructed according to the principles of the present invention.

DETAILED DESCRIPTION

[0018] Interconnects, and more specifically, thick copper surface conductive leads, are well known and commonly used in today's high technology fields. Unfortunately, as recognized by the present invention, as the width of the thick copper surface conductive leads decrease with the use of next generation devices, undercut that exists at the barrier layer/surface conductive lead interface is much more detrimental. The undercut currently effectively reduces the width of the conductive lead at its base by an amount ranging from about 14% to about 30%. While this does not presently cause too many problems, as the desired width of the conductive leads continues to decrease, the undercut could conceivably reduce the width from about 35% to about 70%, or even more if the width of the conductive leads continued to decrease. It is believed that the next generation devices would experience reliability issues due to this extreme undercut.

[0019] One inventive aspect of the present invention is the recognition that the etch chemistries used to etch the barrier layer and copper seed layer located under the conductive leads are at least partially responsible for the undercut. It has further been recognized that the wet etch used to etch the barrier layer actually undercuts the copper seed layer at the barrier layer/conductive lead interface. Given those recognitions and

substantial experimentation, the present invention identified that the wet etch used to etch the barrier layer could be substituted with a dry etch. Uniquely, the barrier layer dry etch does not cause the substantial undercut caused by the barrier layer wet etch. Therefore, in one aspect, the present invention recognizes that a dry etch may be used to etch the barrier layer associated with a conductive lead, to provide a copper lead that does not have the undesirable undercut existing in the prior art devices.

[0020] An additional recognition is the fact that the wet etch also causes undesirable width reduction in the interconnect lead, as well as undesirable oxide formation on the sidewalls of the interconnect lead and the top of the interconnect lead if a protective layer is not used. The dry etch, used in accordance with the principles of the present invention, also substantially eliminates these two undesirable effects.

[0021] Turning now to FIGURE 1, illustrated is a cross-sectional view of one embodiment of an interconnect system 100 manufactured in accordance with the principles of the present invention. The interconnect system 100 of FIGURE 1 initially includes a protective overcoat 110 located over a conductive layer 120. The protective overcoat 110 is often referred to as a passivation layer, and provides electrical isolation and mechanical protection for underlying structures, such as the conductive layer 120. Preferably, the protective overcoat 110 also provides chemical and

ion protection.

[0022] As may be appreciated, the conductive layer 120 may form all or only a portion of a metallization layer. In the embodiment of FIGURE 1, the conductive layer 120 forms a portion of an upper most metallization layer. The conductive layer 120 may comprise one or more different conductive materials, such as aluminum, copper, tungsten, etc.

[0023] Located within an opening in the protective overcoat 110 and contacting the conductive layer 120 is an interconnect 130. The interconnect 130, in an exemplary embodiment of the present invention, provides electrical signals from a source located outside of the protective coating 110 to devices protected by the protective coating 110.

[0024] The interconnect 130 illustrated in FIGURE 1 includes a barrier layer 140 located within the opening and contacting the conductive layer 120. The barrier layer 140, as illustrated, includes a skirt 145 that extends outside a footprint of the surface conductive lead 160. As will be appreciated, the skirt 145 may extend from about 250 nm to about 2000 nm outside of the footprint, and may taper down as it moves away from the surface conductive lead 160. The skirt 145, as will be detailed below, is a result of the unique process used to manufacture the interconnect 130. The skirt 145, however, does provide certain benefits. For example, the skirt 145 provides additional adhesion between the

protective overcoat 110 and the surface conductive lead 160, particularly if an undercut of the seed layer 150 were to occur.

[0025] Located over the barrier layer 140 and at least partially within the opening in the protective overcoat 110 may be a seed layer 150. As those skilled in the art appreciate, the seed layer 150 is used to help electroplate the surface conductive lead 160. In an instance where the surface conductive lead 160 comprises a thick copper surface conductive lead, the seed layer 150 would comprise a copper seed layer.

[0026] The surface conductive lead 160, which may comprise copper or another similar material, may have a number of different widths and thicknesses. Nevertheless, a thickness ranging from about 3 μm to about 25 μm (and commonly from about 6 μm to about 15 μm) and a minimum width comparable to the thickness, are advantageous. Optionally located over the surface conductive lead 160 may be protective layers 170, 180. The protective layer 170 may be a 3000 nm nickel layer and the protective layer 180 may be a 300 nm palladium layer. Other thicknesses and types of materials could comprise the protective layers 170, 180. For example, gold may be used in place of or in conjunction with the palladium layer. It should also be noted that the protective layers 170, 180, not only provide protection, however, those layers also provide an exemplary and robust means of forming the electrical connections, such as wire bonds, to the surface conductive lead 160.

[0027] Turning now to FIGUREs 2-7, illustrated are cross-sectional views of detailed manufacturing steps instructing how one might, in an advantageous embodiment, manufacture an interconnect system similar to the interconnect system 100 depicted in FIGURE 1. FIGURE 2 illustrates a cross-sectional view of a partially completed interconnect system 200. The partially completed interconnect system 200 of FIGURE 2 includes a protective overcoat 210 located over a conductive layer 220. The protective overcoat 210 may comprise one or more layers. Typical layer materials include silicon nitride, silicon oxynitride, silicon oxide, PSG (Phospho-Silicate Glass), organic polymers (e.g., a polyimide), and other materials. Silicon nitride is preferred for its strength, but silicon oxynitride is often used in its place where transparency is needed, for example, to allow UV memory erase. Preferably the overall thickness of the protective overcoat 210 is from about 500 nm to about 2000 nm, more preferable from about 800 nm to about 1500 nm.

[0028] The conductive layer 220, as indicated earlier, may be any conductive material located within an integrated circuit. The conductive layer 220 of the present invention, however, is an upper most metallization layer of the integrated circuit. The conductive material 220 may comprise a number of different materials while staying within the scope of the present invention, including aluminum as it is shown in FIGURE 2.

[0029] An exemplary lithographic process has been used to form an opening 230 in the protective overcoat 210, the opening 230 being located over the conductive material 220. Lithography refers to a process for pattern transfer between various media. The lithographic process may include forming a radiation sensitive resist coating over the layer to be patterned, in this case the protective overcoat 210. The radiation sensitive resist coating may then be patterned by selectively exposing the resist through a mask. In turn, the exposed areas of the coating become either more or less soluble than the unexposed areas, depending on the type of resist. A solvent developer may then be used to remove the less soluble areas leaving the patterned resist. After the resist is patterned, the protective overcoat 210 may be etched using the patterned resist as a mask to transfer the pattern to the protective overcoat 210. Etch processes, among others, might include plasma etching, reactive ion etching, wet etching, or combinations thereof. Nevertheless, plasma etching is preferred. Preferably, the etch process is highly anisotropic and gives vertical sidewalls to the protective overcoat 210. After the opening 230 has been etched in the protective overcoat 210, the remaining resist may be removed, resulting in a device similar to that shown in FIGURE 2.

[0030] Turning now to FIGURE 3, illustrated is a cross-sectional view of the partially completed interconnect system 200 illustrated

in FIGURE 2 after forming a barrier layer 310 over the protective overcoat 210 and within the opening 230. The barrier layer 310 is formed such that it contacts the conductive layer 220 exposed by the opening 230. The barrier layer 310 is conductive, and in an exemplary embodiment limits diffusion from the layers located thereover. In the instant invention the barrier layer 310 prevents copper diffusion from the layers located thereover. Additional functions of the barrier layer 310 can include providing low electrical resistance between the conductive layer 220 and the subsequently formed surface conductive lead, as well as providing good adhesion between these metals. The barrier layer 310 can be a refractory metal such as titanium, tungsten, chromium, molybdenum, or an alloy thereof. In a preferred embodiment, the barrier layer 310 is tungsten titanium (TiW). The thickness of the barrier layer 310 is preferably from about 100 nm to about 500 nm, more preferably from about 200 nm to about 300 nm.

[0031] The barrier layer 310 can be formed by any suitable method including, for example, physical vapor deposition, chemical vapor deposition, electroless plating, electroplating, or sputtering. Generally, chemical or physical vapor deposition may be used to provide uniform coating of the opening 230, especially when the opening 230 has steep sidewalls.

[0032] Turning now to FIGURE 4, illustrated is a cross-sectional view of the partially completed interconnect system 200 illustrated

in FIGURE 3 after forming a seed layer 410 over the barrier layer 310 and within the opening 230. The seed layer 410, in the embodiment of FIGURE 4, is formed such that it contacts the barrier layer 310. The uppermost portion of the seed layer 410 is generally copper. The copper portion is generally from about 100 nm to about 500 nm thick, more preferably from about 200 nm to about 300 nm thick. The seed layer 410 can be deposited by any suitable means including, for example, sputter deposition, chemical vapor deposition or electroplating. It should be appreciated that seed layer 410 in the present example is illustrated as a single layer, however, multi-layer seed layers (*e.g.*, TiW and copper) may be employed and are contemplated by the present invention.

[0033] Turning now to FIGURE 5A, illustrated is a cross-sectional view of the partially completed interconnect system 200 illustrated in FIGURE 4 after patterning a thick resist layer 510 over the protective overcoat 210 and forming a surface conductive lead 520 within an opening patterned in the resist layer 510. The thick resist layer 510 may be patterned using a similar process as discussed above with respect to FIGURE 2. As the thick resist layer 510 will define the shape and thickness of the surface conductive lead 520, the thick resist layer 510 should be deposited to a thickness greater than the desired thickness for surface conductive lead 520. For example, a 25 μm thick resist can be used. The opening patterned within the thick resist layer 510

should range from about 6 μm for narrow leads to several hundreds of μm for wider leads. In next generation devices, however, the width of the opening could be significantly less.

[0034] After patterning the thick resist layer 510, the surface conductive lead 520 may be conventionally plated within the opening in the thick resist layer 510 and on the exposed seed layer 410. As one would appreciate, either electrical or electroless plating can be used. The surface conductive lead 520, in an exemplary embodiment, should have a thickness of at least about 5 μm thick, preferable from about 6 μm to about 15 μm thick.

[0035] Turning briefly to FIGURE 5B, illustrated is a cross-sectional view of an alternative embodiment of the partially completed interconnect system 200 illustrated in FIGURE 5A after forming optional protective layers 530, 540 over the top surface of the surface conductive lead 520. The optional protective layers 530, 540, each have their specific use and material composition. For instance, the protective layer 530 in the embodiment of FIGURE 5B is a 3000 nm nickel layer and is configured to insure reliable wire bonding or for other assembly purposes. In addition, the protective layer 540 in the embodiment of FIGURE 5B is a 300 nm palladium layer configured to protect the surface of the protective layer 530 from unwanted corrosion or oxidation. Similarly, the protective layers 530, 540, provide a surface more acceptable to gold wire bonding. Likewise, the protective layers 530, 540

protect the surface conductive lead 520 from the etchants used to etch the barrier layer 310 and copper seed layer 410.

[0036] Turning now to FIGURE 6, illustrated is a cross-sectional view of the partially completed interconnect system 200 illustrated in FIGURE 5B after removing the thick resist layer 510 and etching the exposed portions of the seed layer 410 to form an etched seed layer 610. As indicated above, those skilled in the art understand the various processes that could be used to remove the thick resist layer 510. The etching of the seed layer 610, however, is a little more unique. In the embodiments of the present invention the seed layer 410 is etched using a wet etch. For instance, a wet etch chemistry including hydrogen peroxide and sulfuric acid has been identified as working extremely well. Other wet etchants are, nonetheless, within the scope of the present invention. Notice how the wet etchant typically used to etch the seed layer 410 does not substantially undercut the etched seed layer 610 or surface conductive lead 520. As the seed layer wet etch is selective to the seed layer 410, it does not substantially affect the barrier layer 310.

[0037] Turning now to FIGURE 7, illustrated is a cross-sectional view of the partially completed interconnect system 200 illustrated in FIGURE 6 after etching portions of the barrier layer 310 extending beyond the surface conductive lead 520 to form a completed interconnect 710. The completed interconnect 710

includes the etched barrier layer 720. Notice again how the etch used to etch the barrier layer 310 does not substantially undercut into the surface conductive lead 520 or etched seed layer 610. Actually, unique to the present invention, the etchant used to form the etched barrier layer 720 often leaves a skirt 725 extending outside a footprint of the surface conductive lead 520. In an exemplary embodiment, the skirt 725 extends from about 250 nm to about 2000 nm outside of the footprint. Additionally, the skirt 725 may taper down as it moves away from the surface conductive lead 520.

[0038] The etchant used to etch the barrier layer 310 is a dry etchant. In an exemplary embodiment the dry etchant includes, amongst other gases, carbon tetrafluoride. As indicated, the carbon tetrafluoride may be combined with a number of different gases and stay within the scope of the present invention. As one would appreciate, each gas has its benefits and drawbacks. For instance, when carbon tetrafluoride is combined with nitrous oxide (N_2O) substantially no undercutting occurs, no oxide forms on the top surface of the surface conductive lead 520 and thus there is no need to perform an addition step to remove this oxide. Additionally, there would be no need to perform an argon plasma clean process to remove any copper that might have been redeposited during the oxide removal step.

[0039] If the carbon tetrafluoride were combined with oxygen,

however, substantially no undercutting would occur, but an oxide layer might form on the top or side surfaces of the surface conductive lead 520. This oxide would therefore need to be removed. In most instances, any copper redeposited when removing the oxide would need to be removed using an argon plasma. Unfortunately, there still exists a chance for DC leakage (e.g., between various completed interconnects 710) and excess capacitance, both of which might cause circuit failures. Nevertheless, the carbon tetrafluoride and oxygen dry etch still provides a superior interconnect 710 to one that might be provided using the conventional wet etch of the barrier layer 310. Carbon tetrafluoride could also be combined with chlorine gas. This combination would again provide substantially no undercut. One skilled in the art will understand the benefits and drawbacks associated with using the chlorine gas.

[0040] Accordingly, it has been observed that a plasma barrier layer etch using about 75 sccm of carbon tetrafluoride and 10 sccm of oxygen at a pressure of about 50 mtorr and energy of about 2500 watts for about 30 minutes provided a superior etched barrier layer 720. Similarly, it has been observed that a plasma barrier layer etch using about 75 sccm of carbon tetrafluoride and 10 sccm of nitrous oxide at a pressure of about 200 mtorr and energy of about 600 watts for about 10 minutes provided a superior etched barrier layer 720. The gas flow rates, pressures, energies and times

previously mentioned could be adjusted and stay within the scope of the present invention.

[0041] Referring finally to FIGURE 8, illustrated is an exemplary cross-sectional view of a conventional integrated circuit (IC) 800 incorporating an interconnect 810 constructed according to the principles of the present invention. The IC 800 may include devices, such as transistors used to form CMOS devices, BiCMOS devices, Bipolar devices, as well as capacitors or other types of devices. The IC 800 may further include passive devices, such as inductors or resistors, or it may also include optical devices or optoelectronic devices. Those skilled in the art are familiar with these various types of devices and their manufacture. In the particular embodiment illustrated in FIGURE 8, the IC 800 includes the interconnect 810. The interconnect 810 is located over dielectric layers 820 having conductive vias 830 located therein.

[0042] Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.